**IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE**

Appl. No. : **10/029,829**

Confirmation No. : **5503**

Applicant(s) : **ZHONG et al.**

Filed : **27 Dec 2001**

TC/A.U. : **2621**

Examiner : **LEE, Y. Young**

Atty. Docket : **US-010719**

Title: **DYNAMIC CONTROL IN COMPLEXITY-CONSTRAINED DATA COMPRESSION**

Mail Stop: **APPEAL BRIEF - PATENTS**
Commissioner for Patents
Alexandria, VA 22313-1450

APPEAL UNDER 37 CFR 41.37

Sir:

This is an appeal from the decision of the Examiner dated 1 June 2006, rejecting claims 1-21 of the subject application, the claims having been at least twice rejected.

This paper includes (each beginning on a separate sheet):

1. **Appeal Brief, with appendices.**

APPEAL BRIEF

I. REAL PARTY IN INTEREST

The above-identified application is assigned, in its entirety, to **Koninklijke Philips Electronics N. V.**

II. RELATED APPEALS AND INTERFERENCES

Appellant is not aware of any co-pending appeal or interference that will directly affect, or be directly affected by, or have any bearing on, the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-21 are pending in the application.

Claims 1-21 stand rejected by the Examiner under 35 U.S.C. 102(b).

Claims 1-16 stand rejected by the Examiner under 35 U.S.C. 103(a).

These rejected claims are the subject of this appeal.

IV. STATUS OF AMENDMENTS

No amendments were filed subsequent to the rejection in the Office Action dated 1 June 2006.

V. SUMMARY OF CLAIMED SUBJECT MATTER

According to one embodiment, the invention addresses control of an encoding process based on a fullness measure of an input buffer (Applicants' specification, page 3, lines 6-11), and has particular application for encoding video data into an MPEG format using a performance-limited encoder, such as a software-based MPEG encoder (page 2, lines 12-17). The encoder is designed to keep-up with the delivery rate of the incoming data (FIG. 4); if the input buffer becomes full, the encoding complexity is decreased (140-150 of FIG. 4); when sufficient buffer space becomes available, the encoding complexity can be increased (160-170 of FIG. 4; page 3, lines 11-19).

As claimed in independent claim 1, one embodiment of the invention comprises a method for encoding a stream of data blocks using a scalable encoder, the method comprising:

receiving a stream of data blocks (page 3, line 7);

storing said received data blocks in an input buffer (14 of FIG. 1; page 3, line 8);

encoding (16 of FIG. 1; 110 of FIG. 4) a first sequence of said stored data blocks from said input buffer to produce a first encoded data block (page 3, lines 8-9);

monitoring (120 of FIG. 4) the fullness level of said input buffer for comparison with a predetermined threshold range to yield an outcome of said comparison (page 3, lines 9-10); and

adjusting (150, 170 of FIG. 4) the complexity of said encoder based on said outcome (page 3, lines 10-11).

As claimed in independent claim 9, one embodiment of the invention comprises a method for encoding a stream of data blocks using a scalable encoder, comprising:

temporarily storing the stream of said data blocks in an input buffer (14 of FIG. 1; page 4, lines 4-5);

retrieving a first sequence of said stored data blocks from said input buffer (page 4, line 5);

encoding (16 of FIG. 1; 110 of FIG. 4) the first sequence of said stored data blocks from said input buffer to produce a first encoded data block (page 4, lines 6-7);

monitoring (120 of FIG. 4) the fullness level of said input buffer (page 4, line 7);

comparing (130 of FIG. 4) the fullness level of said input buffer to a predetermined threshold range (page 4, lines 7-8);

increasing (160-170 of FIG. 4) the complexity of said encoder when the fullness level of said input buffer is below a lower level of said predetermined threshold range (page 4, lines 8-10); and

decreasing (140-150 of FIG. 4) the complexity of said encoder when the fullness level of said input buffer is above an upper level of said predetermined threshold range (page 4, lines 10-11).

As claimed in independent claim 17, one embodiment of the invention comprises an encoding system (FIG. 1) for encoding a stream of datablocks, comprising:

an analog-to-digital converter (12) for converting analog signals from a plurality of sources into digital signals (page 4, lines 20-21);

an input buffer (14) for receiving said converted digital signals at a predefined rate (page 4, lines 21-22);

a memory (20) for storing a predetermined encoding table (page 4, line 22 – page 5, line 1);

an encoder (16) for encoding the stream of data blocks stored in said input buffer (page 5, line 1);

a management module (18), operatively coupled to said input buffer, said encoder, and said memory (page 5, lines 1-2),

wherein said management module is operable to (FIG. 4): (a) receive the stream of said data blocks; (b) store said received data blocks in said input buffer; (c) cause to encode (110) a first sequence of said stored data blocks from said input buffer to produce a first encoded data block; (d) monitor (120) the fullness level of said input buffer for comparison with a predetermined threshold range; (e) cause to adjust (150, 170) the complexity of said encoder based on only said comparison outcome of said input buffer and said predetermined encoding table, said configuration table using a plurality of complexities and encoding options; and, (f) cause to encode (150-110, 170-110) a second data block at said adjusted complexity to produce a second encoded data block (page 5, lines 2-9).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-21 stand rejected under 35 U.S.C. 102(b) over Uz et al. (USP 5,847,761, hereinafter Uz).

Claims 1-16 stand rejected under 35 U.S.C. 103(a) over Ishiyama (USPA 2001/0008544) and Reininger et al. (USP 5,426,463, hereinafter Reininger).

VII. ARGUMENT

Claims 1-21 stand rejected under 35 U.S.C. 102(b) over Uz

MPEP 2131 states:

> "A claim is anticipated only if ***each and every element*** as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The ***identical invention*** must be shown in as ***complete detail*** as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claims 1-8

Claim 1, upon which claims 2-8 depend, claims a method that includes storing received data blocks in an input buffer, encoding a first sequence of the stored data blocks from the input buffer, monitoring the fullness level of the input buffer for comparison with a predetermined threshold range to yield an outcome of said comparison, and adjusting the complexity of the encoder based on the outcome.

Uz fails to teach an input buffer to the encoder, and thus:

Uz fails to teach storing received data blocks in an input buffer;

Uz fails to teach encoding a first sequence of the stored data blocks from the input buffer;

Uz fails to teach monitoring the fullness level of the input buffer; and

Uz fails to teach adjusting the complexity of the encoder based on the outcome of a comparison of the fullness level to a threshold range.

Uz is silent with regard to whether the encoder includes an input buffer. Uz teaches a conventional encoder, wherein the complexity of the encoder is adjusted based on the encoded output. Uz refers to a virtual input buffer (VBF), but this input

buffer is the input buffer that is assumed to exist at the receiving decoder. The MPEG-2 standard states that an MPEG encoder must not create an output that will cause an underflow or overflow at the receiving decoder, and this is the standard that Uz uses to control the encoder (Uz, column 14, line 8 through column 15, line 67).

The Office action of 17 February 2006 asserts that Uz teaches storing received data blocks in a buffer 50'. The applicants respectfully disagree with this assertion. Uz specifically teaches that the buffer 50' is an output buffer of the encoder:

> "The encoder also includes a physical encoder output buffer 50 which is connected to a channel 51 for transmitting the encoded bit stream" (Uz, column 8, lines 28-30), and
> "A portion 50' of the physical encoder buffer 50 is allocated to each master or slave unit 30, 40. In addition, each unit 30, 40 includes a controller 90 in communication with the motion estimation unit 70, encoder unit 80 and physical buffer 50." (Uz, column 8, lines 36-40).

The above passages are the only references to buffer 50 in Uz's disclosure, and therefore an assertion that Uz's "encoder output buffer 50" is an input buffer to the encoder that receives the data to be encoded is unfounded.

Because Uz is silent with regard to an input buffer to the encoder, and fails to teach monitoring a fullness level of an input buffer of an encoder and adjusting the complexity of the encoder based on a comparison to a threshold range, as specifically claimed in claim 1, the applicants respectfully maintain that the rejection of claims 1-8 under 35 U.S.C. 102(b) over Uz is unfounded, per MPEP 2131.

Claims 9-16

Claim 9, upon which claims 10-16 depend, claims a method that includes temporarily storing the stream of the data blocks in an input buffer, retrieving a first sequence of the stored data blocks from the input buffer, encoding the first sequence of the stored data blocks from the input buffer, monitoring the fullness level of the input buffer, comparing the fullness level of the input buffer to a predetermined threshold range, increasing the complexity of the encoder when the fullness level of the input buffer is below a lower level of the predetermined threshold range, and

decreasing the complexity of the encoder when the fullness level of the input buffer is above an upper level of the predetermined threshold range.

As noted above, Uz fails to teach an input buffer to an encoder, and hence the applicants respectfully maintain that Uz fails to teach each of the above cited elements of claim 9.

Because Uz fails to teach temporarily storing the stream of the data blocks in an input buffer, fails to teach retrieving a first sequence of the stored data blocks from the input buffer, fails to teach encoding the first sequence of the stored data blocks from the input buffer, fails to teach monitoring the fullness level of the input buffer, fails to teach comparing the fullness level of the input buffer to a predetermined threshold range, fails to teach increasing the complexity of the encoder when the fullness level of the input buffer is below a lower level of the predetermined threshold range, and fails to teach decreasing the complexity of the encoder when the fullness level of the input buffer is above an upper level of the predetermined threshold range, as specifically claimed in claim 9, the applicants respectfully maintain that the rejection of claims 9-16 under 35 U.S.C. 102(b) over Uz is unfounded, per MPEP 2131.

Claims 17-21

Claim 17, upon which claims 18-21 depend, claims an encoding system that includes an analog-to-digital converter for converting analog signals from a plurality of sources into digital signals, an input_buffer for receiving said converted digital signals at a predefined rate, a memory for storing a predetermined encoding table, an encoder for encoding the stream of data blocks stored in said input buffer, a management module, operatively coupled to said input buffer, said encoder, and said memory, wherein said management module is operable to: (a) receive the stream of said data blocks; (b) store said received data blocks in said input buffer; (c) cause to encode a first sequence of said stored data blocks from said input buffer to produce a first encoded data block; (d) monitor the fullness level of said input buffer for comparison with a predetermined threshold range; (e) cause to adjust the complexity

of said encoder based on only said comparison outcome of said input buffer and said predetermined encoding table, said configuration table using a plurality of complexities and encoding options; and, (f) cause to encode a second data block at said adjusted complexity to produce a second encoded data block.

As noted above, Uz fails to teach an input buffer to an encoder. Additionally, the Office action fails to identify where Uz teaches an analog-to-digital converter for converting analog signals from a plurality of sources into digital signals.

The Board of Patents Appeals and Interferences has consistently upheld the principle that the burden of establishing a prima facie case resides with the Office, and:

> "To meet [the] burden of establishing a prima facie case of anticipation, the examiner must explain how the rejected claims are anticipated by pointing out ***where*** all of the specific limitations recited in the rejected claims are found in the prior art relied upon in the rejection." *Ex Parte Naoya Isoda*, Appeal No. 2005-2289, Application 10/064,508 (BPAI Opinion October 2005).

Because the Office action fails to identify where Uz teaches each of the specific limitations recited in the rejected claims, the applicants respectfully maintain that the Office has not established a prima facie case of anticipation, and thus the rejection of claims 17-21 under 35 U.S.C. 102(b) over Uz is unfounded, per MPEP 2131.

Claims 1-16 stand rejected under 35 U.S.C. 103(a) over Ishiyama and Reininger

The final Office action refers to the Office action dated 20 July 2004 to support the rejection of claims 1-16 under 35 U.S.C. 103(a) over Ishiyama and Reininger; the applicants note that the Office action dated 20 July 2004 rejects claims 1, 2, 4, 6-10, and 12-16 under 35 U.S.C. 102(e) over Ishiyama, and claims 3, 5, and 11 under 35 U.S.C. 103(a) over Ishiyama and Reininger. However, as will be clear from the remarks below, a rejection of these claims under either 35 U.S.C. 102(e) or 103(a) is unfounded, per either MPEP 2131 or 2142.

MPEP 2142 states:

> "To establish a *prima facie* case of obviousness ... the prior art reference (or references when combined) ***must teach or suggest all the claim limitations***... If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness."

Claims 1-8

Claim 1, upon which claims 2-8 depend, claims a method that includes storing received data blocks in an input buffer, encoding a first sequence of the stored data blocks from the input buffer, monitoring the fullness level of the input buffer for comparison with a predetermined threshold range to yield an outcome of said comparison, and adjusting the complexity of the encoder based on the outcome.

Both Ishiyama and Reininger fail to teach or suggest monitoring a fullness level of an input buffer for comparison with a predetermined threshold range to yield an outcome of said comparison, and adjusting the complexity of the encoder based on the outcome.

Ishiyama teaches a decoder-encoder combination that is configured to convert encoded data from one encoded format to another. Ishiyama's decoder 1 receives the original encoded data from a first transmission channel, decodes it into video format, and provides this decoded video to Ishiyama's encoder 2. Ishiyama's encoder 2 encodes the output of the decoder 1 and provides the newly encoded data to a second transmission channel (Ishiyama [0055] and [0069]-[0089]).

Ishiyama teaches an input buffer 21, but this input buffer 21 is an input buffer to Ishiyama's decoder 1. Ishiyama's frame memory 26 may be considered to correspond to an input buffer to Ishiyama's encoder 2, but Ishiyama does not teach a fullness measure associated with this memory 26.

The applicants respectfully maintain that Ishiyama's input buffer 21 does not correspond to the input buffer from which Ishiyama's encoder retrieves "a first sequence of the stored data blocks from the input buffer" as specifically claimed in claim 1.

However, assuming in argument that Ishiyama's input buffer 21 is broadly interpreted as corresponding to an input buffer from which Ishiyama's encoder 2

obtains the sequence of stored data blocks, the applicants further maintain that Ishiyama does not teach or suggest monitoring a fullness level of an input buffer for comparison with a predetermined threshold range to yield an outcome of said comparison, and adjusting the complexity of the encoder based on the outcome, as specifically claimed in claim 1.

Ishiyama teaches controlling the encoding complexity via a quantization step controller 71 based on a monitoring of both the decoder input buffer 21 and the encoder output buffer 40 (Ishiyama [0093]). Ishiyama teaches the conventional control of the encoding complexity based on the fullness of fullness of the encoder output buffer 40 to prevent underflow and overflow (Ishiyama [0094]-[0099]. However Ishiyama's control of the encoder complexity based on the decoder input buffer 21 is not based on fullness per se, and is not based on a comparison of the fullness to a predefined threshold range, as specifically claimed in claim 1.

As Ishiyama teaches at [0027]-[0032], an object of the invention is to optimally utilize the bandwidth (referred to as 'band' in Ishiyama) of the transmit channel relative to the receive channel. As Ishiyama subsequently teaches:

> "if the pre-conversion code volume is larger than the post-conversion code volume, the band[width] of the transmission channel transmitting the bitstream would be not fully utilized. If, conversely, the post-conversion code volume is larger than the pre-conversion code volume, the bitstream cannot be sent with the band[width] of the transmission channel sending out the bitstream, thus causing delay at the output buffer." (Ishiyama [0101].)

At [0100]-[0107], Ishiyama teaches that the volume of the decoder input data (pre-conversion code) is compared to the volume of the encoder output data (post-conversion code) in view of the relative bandwidths of the receive and transmit channels. This comparison of the volume of decoder input data to the volume of encoder output data, appropriately scaled by the ration of receive and transmit bandwidths, is used to adjust the encoding complexity to appropriately increase or decrease the volume of output data.

Even assuming in argument that Ishiyama's volume of decoder input data can be said to correspond to the applicants' claimed fullness level of an encoder input buffer, Ishiyama teaches comparing this volume to the volume of the encoder output data, and not to a threshold range, as specifically claimed in claim 1.

Reininger teaches a multi-frame memory 7 that corresponds to an input buffer to an encoder 8. However, Reininger is silent with regard to a fullness measure associated with this memory 7.

Because both Ishiyama and Reininger fail to teach or suggest monitoring a fullness level of an input buffer for comparison with a predetermined threshold range to yield an outcome of said comparison, and adjusting the complexity of the encoder based on the outcome, as specifically claimed in claim 1, the applicants respectfully maintain that the rejection of claims 1-8 under 35 U.S.C. 103(a) over Ishiyama and Reininger is unfounded, per MPEP 2142.

Claims 9-16

Claim 9, upon which claims 10-16 depend, claims a method that includes monitoring the fullness level of an encoder input buffer, comparing the fullness level of the input buffer to a predetermined threshold range, increasing the complexity of the encoder when the fullness level of the input buffer is below a lower level of the predetermined threshold range, and decreasing the complexity of the encoder when the fullness level of the input buffer is above an upper level of the predetermined threshold range.

As noted above, both Ishiyama and Reininger fail to teach monitoring the fullness level of an encoder input buffer and comparing the fullness level of the input buffer to a predetermined threshold range. As such, the applicants respectfully maintain that the rejection of claims 9-16 under 35 U.S.C. 103(a) over Ishiyama and Reininger is unfounded, per MPEP 2142.

CONCLUSIONS

Because Uz fails to teach an input buffer of an encoder, and thus fails to teach the elements of each of the applicants' independent claims, the applicants respectfully request that the Examiner's rejection of claims 1-21 under 35 U.S.C. 102(b) over Uz be reversed by the Board, and the claims be allowed to pass to issue.

Because both Ishiyama and Reininger fail to teach monitoring the fullness level of an encoder input buffer and comparing the fullness level of the input buffer to a predetermined threshold range, the applicants respectfully request that the Examiner's rejection of claims 1-16 under 35 U.S.C. 103(a) over Ishiyama and Reininger be reversed by the Board, and the claims be allowed to pass to issue.

Respectfully submitted,

Robert M. McDermott, Attorney
Registration Number 41,508
804-493-0707

CLAIMS APPENDIX

1. A method for encoding a stream of data blocks using a scalable encoder, the method comprising:

receiving a stream of data blocks;

storing said received data blocks in an input buffer;

encoding a first sequence of said stored data blocks from said input buffer to produce a first encoded data block;

monitoring the fullness level of said input buffer for comparison with a predetermined threshold range to yield an outcome of said comparison; and

adjusting the complexity of said encoder based on said outcome.

2. The method of claim 1, wherein the step of adjusting the complexity of said encoder based on said comparison outcome comprises:

decreasing the complexity of said encoder when the fullness level of said input buffer exceeds an upper limit of said threshold range; and,

encoding a second data block at the decreased complexity to produce a second encoded data block.

3. The method of claim 2, wherein decreasing the complexity of said encoder is performed according to a predetermined encoding configuration table.

4. The method of claim 1, wherein adjusting the complexity comprises:

increasing the complexity of said encoder when the fullness level of said input buffer is below a lower level of said predetermined threshold range; and,

encoding a second data block at the increased complexity to produce a second encoded data block.

5. The method of claim 4, wherein increasing the complexity of said encoder is performed according to a predetermined encoding configuration table.

6. The method of claim 1, wherein adjusting the complexity comprises maintaining the complexity of said encoder when the fullness level of said input buffer falls within said predetermined threshold range.

7. The method of claim 1, further comprising storing said first encoded data block in a memory medium for subsequent retrieval.

8. The method of claim 1, wherein the stream of data blocks comprises a stream of video frames.

9. A method for encoding a stream of data blocks using a scalable encoder, comprising:

temporarily storing the stream of said data blocks in an input buffer;

retrieving a first sequence of said stored data blocks from said input buffer;

encoding the first sequence of said stored data blocks from said input buffer to produce a first encoded data block;

monitoring the fullness level of said input buffer;

comparing the fullness level of said input buffer to a predetermined threshold range;

increasing the complexity of said encoder when the fullness level of said input buffer is below a lower level of said predetermined threshold range; and

decreasing the complexity of said encoder when the fullness level of said input buffer is above an upper level of said predetermined threshold range.

10. The method of claim 9, further comprising encoding a second data block at the increased complexity to produce a second encoded data block.

11. The method of claim 9, wherein increasing and decreasing the complexity of said encoder are performed according to a predetermined encoding configuration table.

12. The method of claim 9, further comprising encoding a second data block at the decreased complexity to produce a second encoded data block.

13. The method of claim 9, further comprising maintaining the complexity of said encoder when the fullness level of said input buffer falls within said predetermined threshold range.

14. The method of claim 9, further comprising storing said first encoded data block in a memory medium for subsequent retrieval.

15. The method of claim 9, wherein the stream of data blocks comprises a stream of video frames.

16. The method of claim 9, wherein the fullness level of said input buffer is determined based on an input rate of the stream of said data blocks and processing feedback information from said encoder after producing said first encoded data block.

17. An encoding system for encoding a stream of datablocks, comprising:

an analog-to-digital converter for converting analog signals from a plurality of sources into digital signals;

an input_buffer for receiving said converted digital signals at a predefined rate;

a memory for storing a predetermined encoding table;

an encoder for encoding the stream of data blocks stored in said input buffer;

a management module, operatively coupled to said input buffer, said encoder, and said memory,

wherein said management module is operable to: (a) receive the stream of said data blocks; (b) store said received data blocks in said input buffer; (c) cause to

encode a first sequence of said stored data blocks from said input buffer to produce a first encoded data block; (d) monitor the fullness level of said input buffer for comparison with a predetermined threshold range; (e) cause to adjust the complexity of said encoder based on only said comparison outcome of said input buffer and said predetermined encoding table, said configuration table using a plurality of complexities and encoding options; and, (f) cause to encode a second data block at said adjusted complexity to produce a second encoded data block.

18. The system of claim 17, wherein said management module is further operable to decrease the complexity of said encoder when the fullness level of said input buffer exceeds an upper limit of said threshold range.

19. The system of claim 17, wherein said management module is further operable to increase the complexity of said encoder when the fullness level of said input buffer is below a lower level of said predetermined threshold range.

20. The system of claim 17, wherein said management module is further operable to maintain the complexity of said encoder when the fullness level of said input buffer falls within said predetermined threshold range.

21. The system of claim 17, wherein the stream of data blocks comprises a stream of video frames.

EVIDENCE APPENDIX

No evidence has been submitted that is relied upon by the appellant in this appeal.

RELATED PROCEEDINGS APPENDIX

Appellant is not aware of any co-pending appeal or interference which will directly affect or be directly affected by or have any bearing on the Board's decision in the pending appeal.